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SOLS Based Reused Architecture of Fm0/Manchester Encoding

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ABSTRACT: The Intelligent Transportation System in our daily life can be done by DSRC technique. The FMO/Manchester codes reach DC balance by DSRC enhancing signal reliability. Nevertheless, the coding diversity between the FMO and Manchester codes seriously limits the potential to design a fully reused architecture for both. In proposed system SOLS technique is used to overcome this limitation. The hardware utilization rate from both FMO/Manchester can be improved by SOLS technique. FPGA SPARTAN 3XC3S 200 TQ-144 is used to evaluate the performance. The proposed system is implemented using Verilog HDL and simulated by MODELSIM 6.4C synthesized by XILINX tool. The DSRC standards of America Europe and Japan can be fully supported by this encoding capability. The proposed system not only develops fully reused architecture but also exhibits an efficient performance compared with the existing works.

KEYWORDS: Dedicated Short Range Communication (DSRC), Similarity Oriented Logic Simplification (SOLS), Field Programmable Gate Array (FPGA).

I. INTRODUCTION

For the intelligent transportation system like automobile to automobile or automobile to roadside is achieved using the protocol called Dedicated short range communication (DSRC). DSRC enables the message sending and broadcasting as follows.

- (a) For automobile to automobile : safety issues, public information announcement, blind spot intersection warnings, intercars distance, and collision-alarms.
- (b) For automobile to roadside: electronic toll collection (ETC) system and also includes the payment for parking services, gas refueling.

The Fig.1 represents the architecture of DSRC. There are three basic modules in DSRC architecture, they are microprocessor, RF Front-End and baseband processing. For modulation error correction and encoding baseband processing is used. To transmit and receive the wireless signal is done by RF Front-End.

Dc-balance refers to the waveform of transmitted signal and it obtains zero-mean for fast application.

For downlink application both FM0 and Manchester encoding is adopted. SOLS technique is used to propose the fully reused VLSI architecture. Area compact retiming and balance logic-operation sharing are the two core methods of SOLS. Hardware resource to reduce the number of transistors can be done by area-compact timing. FM0 and Manchester encoding can be efficiently combined by balance logic-operation sharing.

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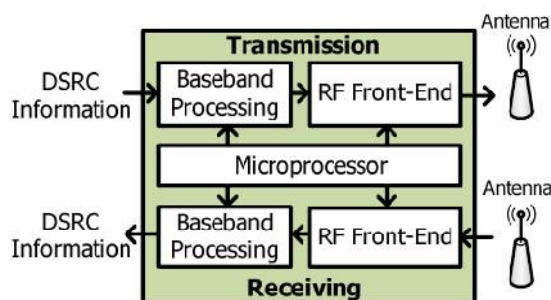


Fig.1 Architecture of DSRC

II. FM0/MANCHESTER CODING RULES

The coding rules for FM0 and Manchester are described as follows.

A.FM0 ENCODING

- (a) The logic 0 represents transition between A and B.
- (b) The logic 1 represents no transition between A and B.
- (c) Among each FM0 code the transition is allocated.

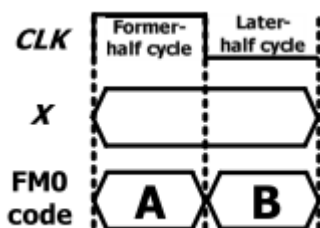


Fig.2 FM0 codeword structure.

As shown in fig.2 the code contains one part for former-half cycle of A and other part for later-half cycle of B.

B. MANCHESTER ENCODING

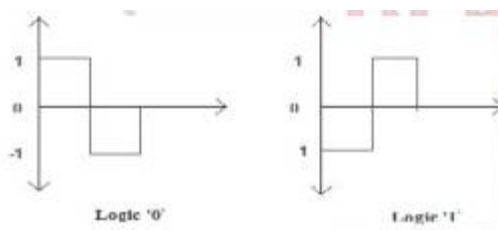


Fig.3 Manchester Encoding

As shown in fig.3 the Manchester encoding is accomplished by following rule

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- (a) Logic 1 represents the transition from low to high.
- (b) Logic 0 represents the transition from high to low.

C. MILLER ENCODING

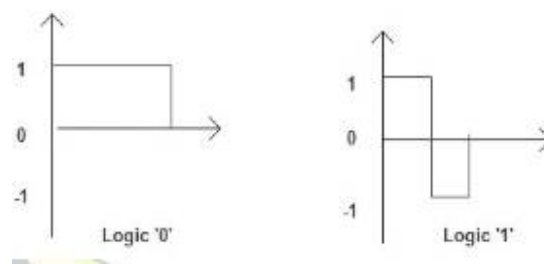


Fig.4 Miller Encoding

As shown in fig.4 the miller encoding is done by following conditions.

- (a) Logic "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period
- (b) Logic "1" causes a transition from one level to the other in the middle of the bit period

III. ANALYSIS ON HARDWARE UTILIZATION OF FM0 AND MANCHESTER ENCODER

The hardware architecture of Manchester encoding is similar to XOR operation. But FM0 encoding is different from Manchester encoding and it is not a simple one. The FM0 encoding architecture starts with FSM as shown in fig.5.

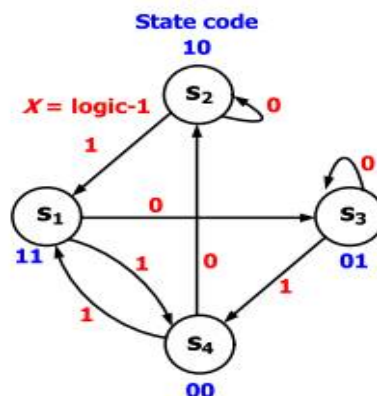


Fig.5 FSM of FM0

The transition table for for FSM of Fm0 is shown in table I. At the time instant t the discrete-time state code of current state is given by A(t) and B(t). Where A(t-1) and B(t-1) represent the previous states. The Boolean functions of A(t) and B(t) are given by

$$A(t) = B(t-1)$$

$$B(t) = X \text{ (xor) } B(t-1)$$

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The Boolean function for FM0 code is given by

$$\text{CLK } A(t) + \text{CLK } B(t)$$

TABLE I
TRANSITION TABLE OF FM0

Previous-state		Current-state			
$A(t-1)$	$B(t-1)$	$A(t)$		$B(t)$	
		$X = 0$	$X = 1$	$X = 0$	$X = 1$
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

With the above 2 equations the hardware architecture of FM0 and Manchester encoding is shown in fig.6. the top part represent the FM0 encoder whereas the bottom part denotes the Manchester encoder. The FM0 encoding depends on the previous state of FM0 code, not only on x. The state code of FM0 is stored in DFF_A and DFF_B. The Mux_1 is used to switch A(t) and B(t) through the selection of CLK. The determination of coding is depends on mode selection of Mux_2.

Mode = 0 ; FM0 code

Mode = 1 ; Manchester code.

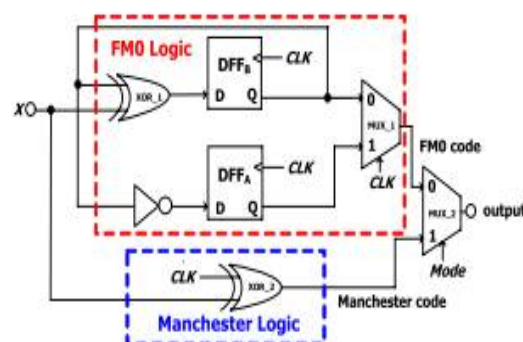


Fig.6 Hardware architecture of FM0 and Manchester encoder

The hardware utilization rate (HUR) is determined by

$$\text{HUR} = \frac{\text{active components}}{\text{Total components}} \times 100\%$$

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The components used for FM0 and Manchester encoding is termed as active component whereas the number of components used in the entire hardware architecture without considering the encoding method is termed as total components.

IV . REUSED ARCHITECTURE DEISGN USING SOLS TECHNIQUE

To design the fully reused VLSI architecture for FM0 and Manchester encoding is the main purpose of SOLS technique. There are two major parts in SOLS technique they are area compact retiming and balance logic operation sharing.

A.AREA COMPACT RETIMING

To derive $A(t)$ and $B(t)$, the boolean functions to be derived must be logic for $A(t)$ and logic for $B(t)$. DFF_A and DFF_B stores the state code for FM0. In fig.7 (a), there occurs a logical fault due to non synchronization between $A(t)$ and $B(t)$ when DFF_A is directly removed. The DFF_B is rearranged such that right after the MUX_1 as shown in fig.7 (b) and its edge is positive triggered. By the help of control signal of the CLK through MUX_1, the FM0 code is switched alternatively. $B(t)$ passes the signal through MUX_1 to the D when the logic is 0.

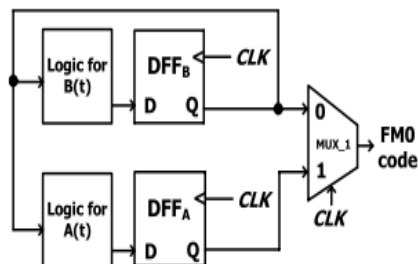


Fig. 7(a) FM0 encoding without area compact retiming

B.BALANCE LOGIC-OPERATION SHARING

As shown in fig.8, the balance logic operation sharing method combines identical logic components of FM0/Manchester encoding. The idea is to integrate X into $A(t)$ and $B(t)$. $A(t)$ can be obtained from inverter of $B(t-1)$. The same inverter is shared by $A(t)/X$ and MUX is placed before the

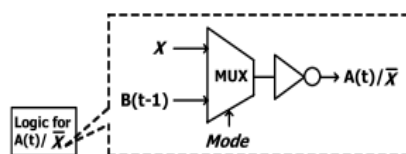


Fig.7 Balance Logic-Operation Sharing

inverter to switch $B(t-1)$ and X operands. The FM0/Manchester encoding is adopted by mode indication. Using above two core concepts of SOLS technique the VLSI architecture of FM0/Manchester encoding is shown in fig.8

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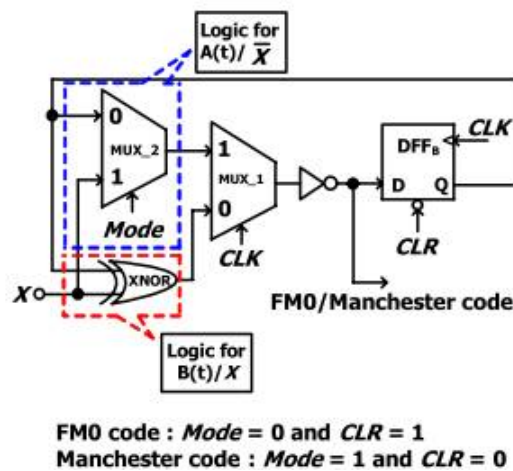


Fig.8 VLSI architecture using SOLS technique

In addition to FM0/Manchester encoding, miller encoding technique is also used in this reused architecture. The modified block diagram is shown in fig.9.

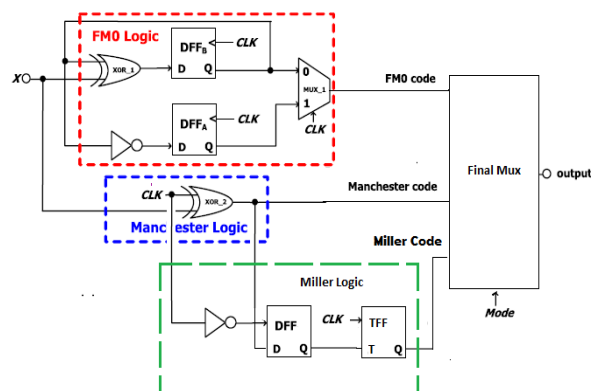


Fig. 9 FM0/Manchester encoding with Miller encoding

V. CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18- μ m 1P6M CMOS technology with an outstanding device efficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is $65.98 \times 30.43 \mu\text{m}^2$. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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